SYSTEM AND METHOD FOR FORCING AN SRAM INTO A KNOWN STATE DURING POWER-UP

ABSTRACT OF THE DISCLOSURE

There is disclosed a static random access memory (SRAM) device that stores an embedded program that is accessible when the SRAM device is powered up. The SRAM device comprises a plurality of storage cells, each of the storage cells comprises a data latch having an input and an output, wherein the data latch comprises a) a first inverter having an input coupled to the first I/O line and an output coupled to the second I/O line, and b) a second inverter having an input coupled to the second I/O line and an output coupled to the first I/O line. The storage cell also comprises a biasing circuit that forces at least one of the first and second I/O lines to a known logic state when power is applied to the SRAM device. The known logic state comprises one bit in the embedded program.